

Appl. No. 10/557,623; Docket No. NL 030534 US
Amdt. dated August 25, 2006
Response to Notice of Non-Compliant Amendment

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Amendments to the Claims

1. (*Currently Amended*) A method of manufacturing an electronic device, in which method at least one field effect transistor (300) is provided on a substrate (301), which provision of the at least one field effect transistor comprises the steps of:

[[-]] applying (201) a patterned first conductor layer (303, 305) on the substrate (301);

[[-]] applying (202) an organic semiconductor layer (307) on the first conductor layer (303, 305);

[[-]] applying (205) a dielectric layer (309) on the semiconductor layer (307);

[[-]] patterning (207) the organic semiconductor layer (307) and the dielectric layer (309) together; and

[[-]] applying (209) a patterned second conductor layer (501) on the patterned dielectric layer (309).

2. (*Currently Amended*) A method as claimed in claim 1 wherein the step of patterning the organic semiconductor layer (307) and the dielectric layer (309) comprises removing the organic semiconductor layer (307) and the dielectric layer (309) from areas not associated with the at least one field effect transistor and from areas not associated with crossing conductors of the first and second conductor layer (303, 305, 501).

3. (*Original*) A method as claimed in claim 2, wherein the said areas associated with a field effect transistor and/or the said areas associated with crossing conductors include protection zones providing a minimal lateral distance between a first conductor in the first conductor layer and a second conductor in the second conductor layer.

4. (*Currently Amended*) A method as claimed in claim 1 wherein the step of applying (202) an organic semiconductor layer on the first conductor layer (303, 305) comprises applying an organic semiconductor or a precursor thereof by spin coating.

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5. (*Currently Amended*) A method as claimed in claim 1 wherein the dielectric layer ~~(309)~~ comprises an initiator sensitive for actinic radiation and functions after irradiation as a mask for the patterning of the semiconductor layer.

6. (*Original*) A method as claimed in claim 4, wherein the dielectric layer comprises a photoresist material.

7. (*Original*) A method as claimed in claim 1, comprising the additional step of providing an electro-optical layer so as to provide a display arrangement.

8. (*Currently Amended*) A method as claimed in claim 6 wherein the substrate ~~(301)~~ is substantially transparent.

9. (*Currently Amended*) An electronic device comprising a plurality of field effect transistor on a substrate ~~(301)~~ and an interconnect structure so as to connect the transistors mutually and/or to an output terminal, the field effect transistors and at least part of the interconnect structure being provided in a stack of:

[[-]] a patterned first conductor layer ~~(303, 305)~~ applied on the substrate;

[[-]] an organic semiconductor ~~(307)~~ layer applied on the first conductor layer ~~(303, 305)~~;

[[-]] a dielectric layer ~~(309)~~ applied on the semiconductor layer ~~(307)~~;

[[-]] a patterned second conductor layer ~~(501)~~ applied on the dielectric layer ~~(309)~~;

[[-]] wherein the semiconductor layer ~~(307)~~ and the dielectric layer ~~(309)~~ are provided in a substantially identical pattern.

10. (*Currently Amended*) An electronic device as claimed in claim 9, wherein the semiconductor layer and the dielectric layer are absent from areas not associated with the field effect transistors and from areas not associated with crossing conductors of the first and second conductor layer ~~(303, 305, 501)~~.